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**Code No: B7701, B6807**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**M.TECH II SEMESTER EXAMINATIONS, APRIL/MAY 2012**
**VLSI TECHNOLOGY & DESIGN**
**(COMMON TO EMEDDED SYSTEMS & VLSI DESIGN, VLSI & EMBEDDED SYSTEMS)**

**Time: 3hours** **Max.Marks:60**

**Answer any five questions**
**All questions carry equal marks**

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1.a) Explain the fabrication process of n-well CMOS technology with neat schematics.
b) Compare CMOS and BiCMOS technologies.

2.a) Explain how threshold voltage depends on fabrication parameters?
b) Determine the ratio of Zpu/Zpd of inverter driving another inverter.
c) What is latch up? How to reduce it?

3.a) What are the λ-based rules for layout?
b) What is meant by bias in VLSI designing?
c) What are the limitations of scaling?

4.a) Draw the circuit diagram of NAND gate in complementary switching logic and explain its working.
b) Why interconnect delay occurs in circuits? How to reduce it?

5.a) What are the different simulations available for combinational circuits?
b) Draw a layout for a two-bit Register and explain its working and also draw its logic diagram.

6.a) Explain two-phase clocking system for sequential circuits.
b) How to optimize a power in sequential circuits. Explain anyone of such techniques.

7.a) Explain a method of placement and routing in floor planning of VLSI design.
b) What do you understand by off-chip connections? How these are designed?

8. Write short notes on:
a) Scheduling and printing
b) Hardware and Software co-design.

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